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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,007	04/18/2001	Mou-Shiung Lin	085027-0042	7677

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McDermott Will & Emery LLP
11682 El Camino Real
Suite 400
San Diego, CA 92130

EXAMINER	
ZARNEKE, DAVID A	

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
11/20/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

SIP_Docket@mwe.com

Office Action Summary	Application No.	Applicant(s)	
	09/837,007	LIN ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *55,57,58,60-62 and 66-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *55,57,58,60-62 and 66-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/27/09 has been entered.

Response to Arguments

Applicant's arguments filed 8/27/09 have been fully considered but they are not persuasive. Two arguments were presented with respect to the rejection of the claims.

First, it is argued that it isn't obvious to use Ti or Ni containing layers in the invention of Nozawa because Farnworth doesn't teach the use of a cylinder and therefore isn't readily applied to the bump of Nozawa because the mechanical considerations and circumstances of each reference are different.

Please note that the references don't have to be exactly the same in order to be combinable. Regardless of the particulars of each reference, the Ti and NI layers of Farnworth are combinable because they both teach the use of bumps in the making of a semiconductor package. In response to applicant's argument that the bumps of Farnworth are nonanalogous art, it has been held that a prior art reference must either

be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, prior art reference must either be in the field of applicant's endeavor. The application of Ni and Ti containing layers of Farnworth readily apply to most any bump regardless of the particulars surrounding that bump, for example whether there is a cylinder underneath of not, because the benefits of these layers aren't dependent upon those particulars, in this case the cylinder.

The second argument is that it isn't obvious to use an underfill in the invention of Nozawa because (1) the polymer layer surrounding the cylinders provide the necessary support, therefore making an underfill unnecessary; and (2) the connecting structure of Nozawa is significantly different than conventional flip-chip bonding.

Please note that while the polymer layer may provide the necessary support, it doesn't provide any other benefit associated with the use of underfills, such as the protection of the bumps from environmental considerations. Further, as noted above, the fact that the structure is different doesn't preclude the benefits of using an underfill. Stated another way, the benefits of using an underfill are not generally dependent upon the surrounding structure, in this case the use of a cylinder.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 13-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, US Patent 6,426,281, in view of Yamai, JP 409045691, and Forehand et al., us Patent 5,847,936, and Mars, US Patent 5,795,818.

Lin teaches a semiconductor device package (figure 17) comprising:

a semiconductor device (30), said device having been provided with points of electrical contact in an active surface thereof (32) , said points of electrical contact

having been provided with fine pitch, high reliability solder bumps (50), said solder bumps extending from said active surface of said semiconductor device over a height of columns of pillar metal (46 & 48), said columns of pillar metal being in contact with said points of electrical contact provided in the active surface of said semiconductor device wherein said pillar metal comprises two metal layers (46 & 48),

While Lin does teach the solder bumps as extending over the pillar metal, but not extending over said pillar metal by at least 0.2 microns, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the distance the solder bump extends over the pillar metal (MPEP 2144.05(b)) because, barring a showing of unexpected results, a skilled artisan would optimize this distance to increase the surface area of the solder bump so that a better connection can be made to the BGA substrate.

Lin fails to teach a Ball Grid Array substrate, said BGA substrate having been provided with points of electrical contact over a first and a second surface thereof, said points of electrical contact provided over the second surface of said BGA substrate being connected to interconnect lines provided over the second surface of said BGA substrate; a solder mask provided over said second surface of said BGA substrate;

said device being positioned over the second surface of said BGA substrate, said fine pitch, high reliability solder bumps facing said second surface of said BGA substrate, providing contact between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said BGA substrate; electrical contact having been established between said fine pitch, high

reliability solder bumps and said points electrical contact provided over said second surface said BGA substrate by a process of solder reflow; said semiconductor device being encapsulated in a molding compound, said molding compound surrounding said device sides including said active surface said device; contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA substrate; and electrical contact having been established between said solder balls inserted into said solder mask provided over said first surface of said BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate by a process of solder reflow.

Yamai teaches a semiconductor device package comprising a BGA substrate (8) having inherent interconnect lines on said surface, said substrate having been provided with inherent points of electrical contact over a first and a second surface thereof, said points of electrical contact provided over the second surface of said substrate', said device being positioned over the second surface of said substrate, said fine pitch, high reliability solder bumps facing said second surface of said substrate (top surface of 8) providing contact between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said substrate; inherent electrical contact having been established between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said substrate', high reliability solder bumps provided to said device comprising an inherent layer of dielectric deposited over the inherent active surface of said device (“chip"), openings having been overlying said points of electrical contact in created in said layer

of dielectric in a pattern an active surface of said device ("chip"), exposing the surface of said points of electrical contact in an active surface of said device; a layer of passivation (3) deposited over the surface of said layer of dielectric, including the exposed surface of said points of electrical contact in an active surface of said device, openings having been created in said layer of passivation in a pattern overlying said points of electrical contact (2) in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device; a layer of metal barrier (4) deposited over the surface of said layer of passivation, including the exposed surface of said points of electrical contact in an active surface of said device; pillar metal (6) and solder bumps (9) overlying said layer of barrier metal in a pattern overlying said points of electrical contact in an active surface of said device, said pillar metal and solder bumps being separated by a layer of under bump metal; and said layer of barrier metal having been etched; said barrier metal having been removed said barrier metal from the surface of said layer of passivation where said barrier layer is not covered by said pillar metal while further leaving in place said barrier layer extending from said pillar metal by a measurable amount.

Yamai does not show that the substrate comprises a solder mask provided over said second surface of said substrate; electrical contact provided over said second surface of said substrate by a process of solder reflow; said semiconductor device being encapsulated in a molding compound, said molding compound surrounding said device on all sides including said active surface of said device', contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA

substrate electrical contact having been established between said solder balls inserted into said solder mask provided over said first surface of said BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate by a process of solder reflow.

However, Mars utilizes a solder mask (601) provided over said second surface of said substrate where said mask removed from a portion of said points of electrical contact provided over the second surface of said BGA substrate by a measurable amount (Column 8, Lines 44-46).

It would have been obvious to one of ordinary skill in the art to incorporate a solder mask over the second surface of said substrate in order to ensure that metallization is applied only to bonding contacts as taught by Mars (Col 8, Lines 45-47).

Forehand discloses a flip chip package (201) with a BGA substrate wherein interconnect lines ("traces") provided over the second surface of said BGA substrate and said semiconductor device is encapsulated in a molding compound (204), said molding compound surrounding said device on all sides including said active surface of said device (Column 2, Lines 49-51); contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA substrate electrical contact having been established between said solder balls inserted into said BGA substrate and said points of solder mask provided over said first surface of said electrical contact provided over said first surface of said BGA substrate.

It would have been obvious to one of ordinary skill in the art to incorporate with the modified package of the Yamai and Mars, an encapsulant by providing a molding

compound surrounding said device on all sides including said active surface of said device or to provide an underfill; and contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA substrate electrical contact having been established between said solder balls inserted into said solder mask provided over said first surface of said BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate, in order to protect the device as is well known in the art.

With respect to claim 13, absent evidence of criticality in the specification the solder balls being fine pitch, would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

With respect to claim 14, neither Yamai, Mars or Forehand appear to explicitly teach the statement of intended use of creating a channel through which cleaning

solution can readily flow, the statement of intended use does not result in a structural difference between the claimed apparatus and the apparatus of the prior ad. Further, because the apparatus is inherently capable of being used for the intended use the statement of intended use does not patentably distinguish the claimed apparatus from the apparatus of prior art. Similarly, the manner in which an apparatus operates is not germane to the issue of patentability of the apparatus; Ex parte Width 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ 2d 1525, 1528 (Fed. Cir. 1990).

With respect to claims 15 and 16, the prior art discloses the claimed invention except for said points of electrical contact provided in an active surface of said device comprising a peripheral pad design or center type pad design.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the points of electrical contact provided in an active surface of said device comprising a peripheral pad design or center type pad design, since it has been held that rearranging parts of an invention involves only routine skill in the art, In re Japikse, 86 USPQ 70 (SSPA 1950).

With respect to claims 19, 20 22, although the prior art does not appear to explicitly disclose the process limitations of "etching said barrier and flux removal from a

gap between said second surface of said BGA substrate and said active surface of said semiconductor device having been performed after completion of flip chip assembly and solder reflow," the product of the prior art inherently possesses the structural characteristics imparted by the process limitation. See In re Fitzgerald, Sanders and Bagheri, 205 USPQ 594 (CCPA 1980).

With respect to claims 21 and 24, the prior art does not explicitly disclose that said points of electrical contact in an active surface of said device have a pitch of about 200 um or less or that said height of columns of pillar metal being between about 10 and 100 pm and more preferably about 50 um.

In any case, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955): In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976)', Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), ced. denied, 469 U.S. 830, 225 USPQ 232 (1984): In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Yamai, Mars and Forehand and further in combination with Pao et al., US Patent 5,931,371.

The prior art does not appear to show dummy solder bumps having been provided over the active surface of said device providing mechanical support for said device, said dummy solder bumps being provided in addition to said fine pitch, high reliability solder bumps provided to said points of electrical contact in the active surface of said device.

However Pao utilizes a dummy solder bump (Fig 4) with fine pitch solder balls.

It would have been obvious to one of ordinary skill in the ad to incorporate dummy solder bumps into the modified package of the prior art in order to improve reliability as taught by Pao (Column 1, Lines 53-57).

As for a claim of bumps, the prior art discloses the claimed invention except for dummy bumps being provided over an active surface. However, it would have been obvious to one of ordinary skill in the art to form bumps, since it has been held that mere duplication of essential working parts involve only routine skill in the art. St Regis Paper Co v. Bemis, 193 USPQ 8 (CA; 1977); see also In re Harza, 124 USPQ 378 (CCPA 1960).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Bryant can be reached on (571)-272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David A. Zarneke/
Primary Examiner, Art Unit 2891
11/17/09